#7A Arndt S Davis 4/17/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: MARTIN A. COTTON

Serial No.:	09/786,787	Group Art Unit:	2841
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For: **NON-CIRCULAR MICRO-VIA**

Commissioner for Patents
Washington, D.C. 20231

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RESPONSE TO OFFICE ACTION UNDER 37 C.F.R. §1.111

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Dear Sir:

In response to the Office Action mailed 03 October 2001, Applicant respectfully requests entry of the following amendment and reconsideration in view of the accompanying remarks.

In the Specification:

Please replace the paragraph spanning pages 7-8 as follows:

-- The advantages of this invention will be better understood by referring to the accompanying drawings, in which **Fig. 1** shows a top view of a typical profile of a power micro-via forming a cross along with a conventional via. **Fig. 2** shows the definition of length and width of a via in a top exterior view using a cross or "+" shaped via. **Fig. 3** shows an alternate Profile-1 forming an elbow or "L" shaped via. **Fig. 4** shows an alternate Profile-2 forming a "U"

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shaped micro via. **Fig. 5** shows an alternate Profile-3 forming a double cross micro via that is not based on a round circular format or where the shape is not centered on the circumference or pitch of a circle diameter. **Fig. 6** shows an alternate Profile-4 forming an "E" shaped micro via that is not based on a round circular format or where the shape is not centered on the circumference or pitch of a circle diameter. **Fig. 7 and Fig. 8** show the Manhattan Interconnect Strategy. **Fig. 9 and Fig. 10** show an alternate guard trench. **Fig. 11 and Fig. 12** show a double guard trench. **Fig 13** shows a cross section of a micro via of the present invention. --

Please insert the following paragraphs at line 7 of page 17.

-- Fig. 13 illustrates a wiring connection structure using a non-circular micro via in accordance with the present invention for a printed circuit board (PCB). To interconnect a plurality of wiring traces applied on different PCB layers, a first wire trace 1302 is applied to a main surface 1300 of the PCB that has a first terminal landing pad 1304 with a first through hole 1306 there through. The first through hole 1306 has a convoluted shaped cross section with a continuous perimeter. A PCB insulation layer 1308 is formed over the first wire trace 1302 and has a second through hole 1310 of identical cross sectional geometry to and vertically aligned with the first through hole 1306, with the second through hole extending to the first terminal landing pad 1304 to expose a portion of it. A second wire trace 1312 is applied to the PCB insulation layer 1308 and has a second terminal landing pad 1314 with a third through hole 1316 that has identical geometry to and is vertically aligned with the first and second through holes 1306, 1310. The first, second and third through holes 1306, 1310, and 1316 are adjoining and are plated there through with an electrically conductive material to form a plated through hole 1318 with a convoluted cross section that vertically intersects the first and second terminal pads 1304

and 1314 and electrically connects the first wire trace 1302 and the second wire trace 1312 by a connection between the first and second wire trace terminal landing pads 1304 and 1314 and the plated through hole 1318. The through holes have any non-circular shape disclosed in Figs. 1-7, such as a shaped continuous curved cross section centered on a circumference diameter of a standard single diameter circular profile, wherein the continuous curved cross section can be "U" shaped, "L" shaped, "+" shaped, or can beyond the perimeter defined by the circumference diameter.

A2 (cont'd)

The wiring connection of fig. 13 is also exemplary of the structure and methods used by the traces, landing pads, and vias illustrated in Fig. 8. --

Please replace the paragraph spanning lines 8-24 of page 14 as follows:

-- The micro milled trenched is a third form for using the micro via concept of having a non-circular or round cross section. Trenching is a slot that is "micro milled" using plasma or laser processing or other method if removing away material about a centerline. This slot is greater in depth than one layer. Trenching is similar to the 1D-3D via formats shown previously. The difference between 1D-3D vias and trenching is length, the vias with a larger ratio than 3.0 : 1.0 is for this patent called trenching. This does not mean that the two are not interchangeable. There will be instances where the trenching could possibly be smaller than a ratio of 3D, such as the case of a trench having a length greater than two times a breath of the trench, so this must be taken into consideration for this invention. Trenching can be used for EIVIC screening but this technique can be used for all known reference plane or screening techniques that control signal integrity in laminate interconnect solutions. This trenching can be used on the edge of PCB's or within the area of the PCB. Trenching can be used in all PCB or application specific module

A3

A3 (end)

types, It offers significant signal performance increases, but at a potentially lower layer count and hence lower production costs. --

In the Drawings:

Please approve and enter the proposed new drawing Fig. 13, as shown in the attached Proposed Drawing Correction.

In the Claims:

Please amend the claims as follows:

9. (Amended) A reference plane structure of a printed circuit board for fixing a potential reference for a plurality of wiring circuit trace layers that are electrically isolated there between by a plurality of printed circuit board layers and having a printed circuit board first layer with a main surface, characterized by:

a first wire trace circuit layer applied to said main surface;

A4

a first printed circuit board-insulating layer formed over said first wire trace circuit layer;

a first reference plane applied over the first printed circuit board insulation layer;

a trench having an interior wall and extending about a perimeter encompassing the first wire trace circuit layer and extending through the printed circuit board first layer, extending through and exposing the first wire trace circuit layer, extending through the first insulation layer and extending to the reference plane exposing said reference plane; and

a conductive plating layer on the interior wall electrically connecting the first wire

trace layer to the grounding plane.

27. (New) The wiring connection structure of claim 3, wherein said convoluted shaped cross section is a square.

28. (New) The method of interconnecting a plurality of wire traces of claim 17, wherein translating the cutting means forms a square.

REMARKS

Claims 1-26 remain in the application. New claims 27-28 has been added to more clearly claim the via structure of Fig. 6A. New figure 13 and associated text have been added to support claims 3, 13, 16, and 17. No new matter has been added.

Drawings Objections

The drawings were objected to under 37 CFR 1.83(a) because "the trench having a length greater than two times a breath of the trench" of claim 2 was purportedly not illustrated. However, Applicant submits that this feature is illustrated sufficiently in figure 9 (see 902) and figure 11 (see 1100, 1102).

The drawings were additionally objected to because "the recited feature of claims 3, 13, 16-17 such as 'a first wire trace applied to main surface ... a connection between the first and second wire trace terminal landing pads and the plated through hole'" were not illustrated. New figure 13 has been submitted to illustrate these claimed elements.

Applicant submits that the drawings now comply with 37 CFR 1.83(a).

Objections to the Specification

The specification was objected to "as failing to provide proper antecedent basis for the

claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01 (o)" because "the specification does not support the limitation "the trench having a length greater than two times a breath of the trench", as recited in claim 2" nor "the limitations of claims 3, 13 and 16-17 (i.e. a first wire trace having a first through hole, a printed circuit board first insulation layer formed over the first wire trace having second through hole, a second wire trace applied to the insulation layer having a second terminal landing pad with a third through hole having identical geometry to and vertically aligned with the first and second through holes)."

The specification has been amended herein to address both of these objections, and Applicant submits that the specification is now incompliance with 37 CFR 1.75(d)(1).

Claim Rejections - 35 USC §112

Claim 9 was rejected under 35 USC 112 as being indefinite since the limitation to "the ground plane" lacked a proper antecedent basis in the claims. Claim 9 has been amended to change "the" to --a--. Applicant therefore submits the term no longer requires an antecedent and the claim is definite.

Claim Rejections - 35 USC §102

Sen et al.

Claims 1, 3-4, and 13-17 were rejected under 35 U.S.C. 102(b) as being anticipated by Sen et al. (US 5,414,222). However, to anticipate a claim, the reference must teach every element of the claim:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must

be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In the present case, claim 1 is drawn to a completely different kind of via than the via disclosed in Sen et al. in that it claims "a wiring connection structure for ***a printed circuit board*** for interconnecting wiring circuit traces on a plurality of circuit trace layers applied on **a *plurality of printed circuit board layers*** and electrically isolated there between by the ***printed circuit board layers*** and ***having a printed circuit board multi-layer structure***, characterized by: ***a through hole*** with a convoluted shaped cross section ***having an interior wall*** that vertically extends through and intersects and exposes a plurality of wire circuit traces and ***having a plating of conductive material applied to the interior wall*** electrically connecting a plurality of wire exposed circuit traces on a plurality of circuit layers." Claims 3, 13, and 16 similarly include claim limitations that include ***printed circuit boards*** with ***plated*** through holes.

Whereas the present invention claims a ***hollow*** type of via used in PCBs that is formed by ***plating*** a through hole, Sen et al. discloses a ***solid*** type of via used in semiconductors that is formed by ***filling*** a through hole (see column 3, lines 15-22, wherein Sen et al. discusses that the "via is solid."). Applicant's disclosure discusses the differences between semiconductor vias and vias of the present invention from page 4, line 12 to page 5, line 17.

The only mention of PCBs in Sen et al. is a discussion of *materials, not structures,* at column 2, lines 26-32, wherein it states that the Sen et al. invention is not meant to be "limited to ceramic packaging only, but is applicable to packaging using...PCB *materials* such as FR4...".

In view of this, Applicant submits that the Office Action is erroneous where it states

- "Sen et al. disclose ... a wiring connection structure for ***printed circuit board***,

characterized by ... a ***plating of conductive material*** ..." with respect to claim 1;

- " Sen et al. disclose... ***a printed circuit board first insulating layer (20)***... and second wire circuit trace (21) applied to ***the printed circuit board***... wherein the first, second and third through holes are adjoining and ***are plated there through with an electrically conductive material forming a plated through hole***..." with respect to claims 3-4,13, and 16; and
- " the method of manufacturing would be ***inherent to the shown structure***" of Sen et al. with respect to claim 17.

With respect to claims 1, 3-4, 13, and 16, the Office Action further invoked *Ex parte Masham*, 2USPQ F.2d 1647 (1987), which held "that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" to somehow "satisfy[ing] the claimed structural limitations pertaining to [sic] phrase 'for interconnecting wiring circuit traces on a plurality of circuit trace layers applied on a plurality of printed circuit board layers and electrically isolated there between by the printed circuit board layers and having a printed circuit board multi-layered structure'."

However, as clearly stated in M.P.E.P. §2114, *Ex parte Masham* only applies "***if the prior art apparatus teaches all the structural limitations of the claim***" and Sen et al. does not teach all the structural limitations with respect to hollow PCB vias employing ***plating***, as discussed above. Indeed, Applicant respectfully submits that the proper portion of the M.P.E.P. for evaluating the printed circuit board limitations in the preamble is §2111.02 discussing that "any terminology in the preamble that limits the structure must be treated as a claim limitation."

In view of these differences, Applicant submits that Sen et al. fails to teach or fairly

suggest the invention of claims 1, 3-4, and 13-17 and respectfully requests reconsideration and allowance of the claims.

Harada et al.

Claims 2, 9-12, 20-23 were rejected under 35 U.S.C. 102(e) as being anticipated by Harada et al. (US 5,966,294).

However, the only portion of Harada et al. referred to in all of these rejections is FIG. 3, which is described in Harada et al. as follows: "FIG. 3 illustrates a multi-layered printed circuit board suggested in Japanese Unexamined Utility Model Publication No. 5-76083. The suggested printed circuit board 111 includes a pair of outer surface layers 140, and signal pattern layers 141a, 141b, 141c and 141d formed between the outer surface layers 140. The outer surface layers 140 are designed to have a ground pattern or a solid pattern in order to act as a shield, thereby preventing emission of electromagnetic waves from the signal pattern layers 141a to 141d."

FIG. 3 of Harada et al. fails to teach or suggest ***any*** form of trench, let alone Applicant's claimed structure and process, such that claims 2, 9-12, and 20-23 are clearly not taught or fairly suggested by Harada et al. In view of this, Applicant therefore respectfully requests reconsideration and allowance of the claims.

Furthermore, from the Office Action comments regarding the alleged failure to illustrate the trench of claim 9 (illustrated in figures 9-12) and the misapplication of Harada et al. as an anticipatory reference, it appears that the Examiner may have failed to adequately comprehend the structure and operation of this aspect of Applicant's invention, which is more fully explained with reference to figures 9-12 and the accompanying text.

Claim Rejections - 35 USC §103

Claims 3-4 were [alternatively] rejected under 35 U.S.C. 103(a) as being unpatentable over Kamperman et al. (US 5,734,5601) in view of Sen et al.

Kamperman et al. is drawn to a cap for attaching a chip or other device to a multi-layer electronic structure (i.e., a printed circuit board). The cap includes a plurality of pads of an electrically-conducting material attached over plated through holes (vias) of the multi-layer electronic structure. Each of the pads includes a flat upper surface for attaching the chip or other device to the multi-layer structure, provides an electrical connection between the chip or other device and the multi-layer structure, and seals the through holes (vias) to prevent solder from entering the plated through hole. The pads are physically isolated from each other.

As a whole, Kamperman et al. teaches against any filling of the vias (see also column 1, line 51 to column 2, line 16 discussing the problems with prior art filled through holes) and fails to suggest any reason to modify the vias. The Kamperman et al. patent also fails to mention wires or traces as suggested by the examiner's mark-up of figure 2 and does not deal with any inductance issues. Sen et al., as discussed above, is drawn to filled vias for semiconductor-type applications and fails to teach or suggest any usability in the form of a hollow, plated through hole.

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. (See M.P.E.P. Section 2143).

The stated reason in the Office Action to combine Kamperman et al. and Sen et al. was

"in order to have a characteristic inductance property", whatever that might mean, since it is ***prior art circular vias*** that have characteristic inductance.

Applicant submits that this stated reason to combine is improper hindsight for the following reason. Sen et al. is concerned with ***parasitic inductance between leads***, and seeks to reduce it by shortening leads (see column 3, lines 42-47: "The via shape allows the via to be placed much closer to the end of a lead, such as those for power and ground, compared to multiple parallel-connected vias. This ***shortening of lead lengths*** reduces inductance which permits an integrated circuit package with higher performance.")

The present invention is drawn to reducing a different property, the ***characteristic inductance of hollow, circular vias caused by the spiraling travel of electrons in a plated circular via***. Since this property does not exist in the filled vias of Sen et al., it is unclear why one of ordinary skill in the art would look to Sen et al. to solve a different problem that has only been disclosed in Applicant's disclosure.

For the above reasons, Applicant submits that claims 3-4, as well as claims 5-8, which also rely on the above combination of Kamperman et al. and Sen et al., are not taught or fairly suggested by the prior art, and Applicant respectfully requests reconsideration.

The obviousness rejection of claims 18-19 relies on Sen et al., which has already been shown above to lack more than laser ablation such that the rejection fails for the same reasons cited above with respect to 35 USC 102.

Likewise, the obviousness rejection of claims 24-26 relies on Harada et al., which has already been shown above to lack any disclosure to trenches such that the rejection fails for the same reasons cited above with respect to 35 USC 102.

For the above reasons, Applicant submits that claims 18-19 and 24-26 are not taught or fairly suggested by the prior art and respectfully requests reconsideration.

Conclusion

For the reasons cited above, Applicants submit that claims 1-16 and 19-25 are in condition for allowance and requests reconsideration of the application. If there remain any issues that may be disposed of via a telephonic interview, the Examiner is kindly invited to contact the undersigned at the local exchange given below.

Respectfully submitted,

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